

INFORMATION DISCLOSURE CITATION PTO-1449	CUSTOMER NUMBER 26615	ATTORNEY'S DKT No. H1415	APPLICATION No. Unassigned 10/726 508
		APPLICANT(S) Wiley Eugene HILL et al.	
		FILING DATE December 4, 2003	GROUP Unassigned 2818

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE

FOREIGN PATENT DOCUMENTS

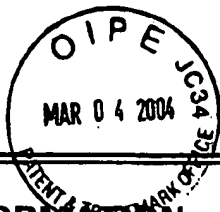
EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						Yes	No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

THP	Digh Hisamoto et al., "FinFET-A Self-Aligned Double-Gate MOSFET Scalable to 20 nm," IEEE Transactions on Electron Devices, Vol. 47, No. 12, December 2000, pages 2320-2325.
	Yang-Kyu Choi et al., "Sub-20nm CMOS FinFET Technologies," 2001 IEEE, IEDM, pages 421-424.
	Xuejue Huang et al., "Sub-50 nm P-Channel FinFET," IEEE Transactions on Electron Devices, Vol. 48, No. 5, May 2001, pages 880-886.
	Xuejue Huang et al., "Sub 50-nm FinFET: PMOS," 1999 IEEE, IEDM, pages 67-70.
THP	Yang-Kyu Choi et al., "Nanoscale CMOS Spacer FinFET for the Terabit Era," IEEE Electron Device Letters, Vol. 23, No. 1, January 2002, pages 25-27.

EXAMINER THP-THP-10	DATE CONSIDERED Aug 2004
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TH	Copy of co-pending U.S. Patent Application No. 10/459,576; by Yider Wu et al., filed June 12, 2003 entitled: "Non-Volatile Memory Device," 20 page specification, 11 sheets of drawings.						
EXAMINER TH-TU+10				DATE CONSIDERED Aug 2004			

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